

AMENDMENTS TO THE CLAIMS

The following listing of claims replaces all prior versions of the claims and all prior listings of the claims in the present application.

1. (currently amended) A demodulation circuit for a digital television receiving system, comprising:

a polyphase filter for converting a data rate of a digital intermediate frequency signal into a desired data rate of the digital intermediate frequency signal in response to an address selection signal, and for dividing and outputting the digital intermediate frequency signal into a first signal having a real number component and a second signal having an imaginary number component;

a complex multiplication unit for multiplying the first and second signals by a complex sinewave obtained from a restored carrier so as to remove frequency offsets from the first and second signals, and for generating a first baseband signal and a second baseband signal as [[the]] a result of removing the frequency offsets;

a carrier restoration circuit for detecting the frequency offsets of the carrier from the first and second baseband signals and for generating the complex sinewave that is proportional to the frequency offsets;

a matched filter for filtering the first and second baseband signals to control signal-to-noise ratios thereof;

a sort circuit for shifting [[the]] frequencies of outputs from the matched filter;

a direct current (DC) removal circuit that combines [[the]] outputs of the sort circuit and removes a direct current component from [[the]] a result of the combination;

a sampling rate control circuit for changing [[the]] a sampling rate of an output of the DC removal circuit and for outputting the result; and

a symbol timing restoration (STR) circuit for measuring a timing error in related symbols of the output of the DC removal circuit and for generating the address selection signal that is proportional to the timing error, in response to a carrier restoration signal that is generated by the carrier restoration circuit and for indicating restoration of the carrier.

2. (currently amended) The demodulation circuit of claim 1, wherein the sort circuit lowers the frequency of the outputs [[of]] from the matched filter.

3. (currently amended) The demodulation circuit of claim 1, wherein the DC removal circuit comprises:

a first subtracter for subtracting the second baseband signal, the second baseband signal having a frequency shifted by the sort circuit, from the first baseband signal, the first baseband signal also having a frequency ~~being also~~ shifted by the sort circuit;

a DC component restoration circuit for detecting a DC component from an output of the first subtracter; and

a second subtracter for subtracting an output of the DC component restoration circuit from the output of the first subtracter.

4. (original) The demodulation circuit of claim 1, wherein the sampling rate control circuit reduces the sampling rate of the output of the DC removal circuit by at least a half.

5. (currently amended) The demodulation circuit of claim 1, wherein the STR circuit comprises:

a timing error detector for detecting ~~the~~ timing error ~~from~~ of the output of the DC removal circuit;

a multi low pass filter (LPF) for removing a high frequency component from the timing error output from the timing error detector; and

a polyphase filter (PPF) controller for receiving an output of the multi LPF and for outputting the address selection signal, in response to the carrier restoration signal.

6. (currently amended) The demodulation circuit of claim 5, wherein the multi LPF removes ~~the~~ high frequency component ~~from~~ of the timing error by changing the bandwidth of the multi LPF.

7. (original) The demodulation circuit of claim 1, wherein symbol synchronization is performed by the STR circuit after restoration of the carrier by the carrier restoration circuit.

8. (currently amended) The demodulation circuit of claim 1, wherein the first signal is an in-phase (I) signal and the second signal is a ~~quadrature (Q)~~ quadrature-phase (Q) signal.

9. (currently amended) A method of demodulating a received signal, comprising:

converting a data rate of a digital intermediate frequency (IF) signal into a desired data rate of the intermediate frequency signal in response to an address selection signal;

dividing and outputting the digital IF signal into a first signal with a real number component and a second signal with an imaginary number component;

multiplying the first and second signals by a complex sinewave obtained from a carrier so as to remove frequency offsets from the first and second signals and generating a first baseband signal and a second baseband signal as ~~[[the]]~~ a result of removing the frequency offsets;

receiving the first and second baseband signals, controlling their signal-to-noise ratios (SNRs), and shifting [[the]] frequency bands of the SNR-controlled first and second baseband signals;

combining the frequency-shifted first and second baseband signals and removing a direct current (DC) component from a signal obtained therefrom;

changing and outputting [[the]] a sampling rate of the signal obtained in the combining step;

receiving the first and second baseband signals, detecting [[the]] frequency offsets from the carrier, and generating the complex sinewave that is proportional to the frequency offsets; and

receiving the signal obtained in the combining step and generating the address selection signal, in response to a carrier restoration signal that indicates restoration of the carrier.

10. (original) The method of claim 9, wherein receiving the first and second baseband signals further includes lowering the frequency bands of the controlled first and second baseband signals.

11. (currently amended) The method of claim 9, wherein the combining step further includes:

subtracting the frequency-shifted second baseband signal from the frequency-shifted first baseband signal;

detecting the ~~direct-current~~ DC component from ~~[[the]]~~ a result of the subtraction; and

subtracting the result of the detection from the result of the subtraction.

12. (currently amended) The method of claim 9, wherein the step of changing and ~~multiplying~~ outputting includes reducing by half the sampling rate of the ~~result~~ signal obtained in the combining step.

13. (currently amended) The method of claim 9, wherein the step of receiving the signal further includes:

receiving the ~~result~~ signal obtained in the combining step and detecting a timing error from the received ~~result~~ signal;

removing a high frequency component from the timing error obtained in the receiving step hereof using a multi low pass filter (LPF); and

receiving ~~[[the]]~~ a result obtained in removing step hereof and outputting the address selection signal, in response to the carrier restoration signal.

14. (currently amended) The method of claim 13, wherein the multi LPF removes the high frequency component from the timing error by changing ~~[[the]]~~ a bandwidth of ~~[[a]]~~ the multi LPF.

15. (currently amended) The method of claim 9, wherein the first signal is an in-phase (I) signal and the second signal is a ~~quadrature (Q)~~ quadrature- phase (Q) signal.

16-24. (canceled)